NOISE MARGIN ANALYSIS OF A-SI:H DIGITAL CIRCUITS AND INTEGRATED A-SI:H ROW DRIVERS ON STAINLESS STEEL SUBSTRATES

by

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ABSTRACT

Amorphous silicon (a-Si) thin film transistors (TFT) on glass is the dominant technology for the active matrix backplane in flat panel displays, and digital radiography. Recently, amorphous silicon thin film transistors have been fabricated on flexible substrates including plastic and stainless steel enabling a variety of new applications. Both reflective and emissive flexible displays have been built, and a small volume production facility for flexible a-Si backplanes is being established. For flexible display and flexible electronic demands, more reliable flexible circuits are required. In this thesis, the lifetime of flexible digital circuits are addressed by analyzing the noise margin. The noise margin is one of the fundamental metrics to evaluate the viability and robustness of digital circuits. An analytical model of amorphous silicon digital circuit noise margin is developed, including the effects of circuit aging. The threshold voltage of a-Si:H transistors increases over time with electrical stress, degrading the performance and eventually leading to circuit wear-out. Since static & dynamic inverters are the basic digital circuit design elements, they are the basis for this analysis. The analytical model is verified with experimental measurements. This thesis also discusses various flexible row driver designs and compares flexible row drivers in terms of lifetime, speed, power consumption and circuit complexity.

To

My Family

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