Circuit Simulation of Threshold-Voltage Degradation in a-Si:H TFTs Fabricated at 175 °C

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***Abstract*—This brief presents a novel approach to modeling gate bias-induced threshold-voltage (V_{th}) degradation in hydrogenated amorphous silicon thin-film transistors (TFTs). The V_{th} degradation model is added to the SPICE 3.0 TFT device model to obtain a composite model and is verified by comparing the simulated V_{th} shift with measured data in a TFT latch circuit.**

***Index Terms*—Circuit simulation, display technology, hydrogenated amorphous silicon thin-film transistor (a-Si:H TFT), SPICE, threshold-voltage degradation.**

I. Introduction

Analytical models based on the physics of hydrogenated amorphous silicon thin-film transistor (a-Si:H TFT) operation that were developed for circuit simulators are able to capture the static and dynamic behaviors of TFTs but ignore time-dependent instabilities caused by gate voltage (V_{GS}) stress [1]. This brief begins by describing the physics behind the V_{th} degradation phenomenon and the subsequent incorporation of a semiempirical V_{th} shift model inside SPICE 3.0 in Section II. In Section III, the simulation results obtained using the combined ΔV_{th} TFT model are compared with the measured V_{th} shift results of an n-channel TFT latch circuit fabricated with a low temperature (175 °C) process. Conclusions are summarized in Section IV.

II. ΔV_{th} Circuit Equivalent Model

The two mechanisms that are responsible for the V_{th} degradation in a-Si:H TFTs are 1) charge injection in the silicon nitride (SiN_x) gate insulator and 2) creation of defect states in the a-Si:H conducting channel [2]. Charge injection in the SiN_x gate is mainly due to tunneling of carriers from extended states in the a-Si:H layer to the trap states in the nitride [3]. These charges are assumed to be located at the SiN_x/a-Si:H interface and add to the fixed charges in the insulator thereby shifting V_{th}. Subsequently, field-effect experiments have provided evidence [2], [4] that mobile carriers are responsible for breaking the weak Si–H bonds resulting in the creation of charged defect states (dangling bonds). Hence, the density of created defect states is proportional to the number of mobile carriers, which affects the Fermi level position resulting in a V_{th} shift. The dominance of any one mechanism is dependent on the stress conditions. Under low to medium positive V_{GS} stress, defect creation is dominant, whereas for negative V_{GS}, charge trapping is the dominant instability mechanism. From the V_{th} shift measurements made on a 96 μm/9 μm n-channel TFT (see Fig. 1), a time-dependent semiempirical equation of ΔV_{th} is given by

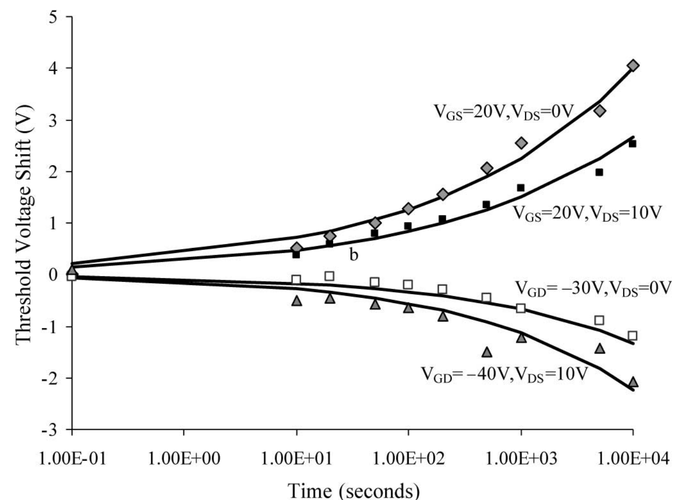

Fig. 1. ΔV_{th} versus stress time of a 96 μm/9 μm n-channel TFT at $V_{\mathrm{GS}} = 20$ V with $V_{\mathrm{DS}} = 0$ V and $V_{\mathrm{DS}} = 10$ V, $V_{\mathrm{GD}} = -30$ V with $V_{\mathrm{DS}} = 0$ V, and $V_{\mathrm{GD}} = -40$ V with $V_{\mathrm{DS}} = 10$ V.

$$\Delta V_{\mathrm{th}}(t) = A \cdot \exp\left(-\frac{E_A}{kT}\right) \cdot t^{\beta}(V_{\mathrm{GS}} - \eta V_{\mathrm{DS}} - V_{\mathrm{th},0})^n. \tag{1}$$

Here, k is the Boltzmann constant, T is the absolute temperature, t is the bias stress time duration, E_A is the mean activation energy, A is the degradation rate, and β and n are process-related constants. The additional V_{DS} term in (1) is attributed to the decrease in mobile carriers at the SiN_x/a-Si:H interface when the TFT enters saturation. Alternate expressions for ΔV_{th} that are comparable to (1) have been reported [5]–[7].

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Using nonlinear least squares estimation [8], the measured V_{th} shift curves from Fig. 1 are fitted to (1) giving $Ae^{(-E_A/kT)} = 0.025$, $n = 1.0$, and $\beta = 0.25$ for the positive shift $[\Delta V_{\text{th}}(+)]$ caused as a result of $V_{\text{GS}} > 0$. The magnitude of ΔV_{th} when $V_{\text{DS}} > 0$ is corrected by $\eta \cdot V_{\text{DS}}$, where $\eta = V_{\text{GS}}/(V_{\text{GS}} + V_{\text{DS}})$. Subsequently, $Ae^{(-E_A/kT)} = 0.0025$, $n = 1.1$, and $\beta = 0.29$ for the negative shift $[\Delta V_{\text{th}}(+)]$ when $V_{\text{GS}} < 0$, the parameter η is computed as before. The lower value of $Ae^{(-E_A/kT)}$ for $V_{\text{GS}} < 0$ is due to the higher hole, versus electron, activation energy. The V_{th} of the unstressed n-channel TFT under test is 5 V. The higher percentage of V_{th} shift (which is more than 75% when stressed for 3 h at $V_{\text{GS}} = 20$ V) is because the n-channel a-Si:H TFTs are fabricated at a 175 °C low temperature process that is compatible with flexible transparent substrates [9].

To quantitatively predict the degradation that each transistor suffers, an equivalent circuit model for ΔV_{th} has been developed. Due to the nonlinear nature of (1), an intermediate parameter "Age" is introduced. Note that Age is a linear function of the bias stress time. The Age parameter provides the means to quantify the degradation suffered by individual TFTs in the circuit and is related to ΔV_{th} by

$$\Delta Age(\Delta t_i) = \int_{t_{i-1}}^{t_i} A^{-\beta} \exp\left(\frac{-E_A}{\beta kT}\right) \cdot (V_{\text{GS}} - \eta V_{\text{DS}} - V_{\text{th},0})^{\frac{n}{\beta}} dt \tag{2}$$

where V_{GS} and V_{DS} are assumed constant during $\Delta t_i = t_i - t_{i-1}$. The incremental Age's (ΔAge) are summed to obtain the total Age at the end of the simulation time (t_{stop}), i.e.,

$$Age \equiv Age(t_{\text{stop}}) = \sum_{i=0}^{N} \Delta Age(\Delta t_i). \tag{3}$$

Finally, Age and ΔV_{th} are extrapolated to a user-specified poststress circuit age (t_{age}), assuming that the stimulus applied over time to the total Age can be approximated by a periodic application of the stimulus used in (2) by applying

$$\left.\begin{aligned} Age(t_{\text{age}}) &= \frac{t_{\text{age}}}{t_{\text{stop}}} Age(t_{\text{stop}}) \\ \Delta V_{\text{th}}(t_{\text{age}}) &= [Age(t_{\text{age}})]^{\beta} \end{aligned}\right\}. \tag{4}$$

To determine the poststress circuit behavior, the simulation is repeated with the extrapolated ΔV_{th}. The ΔV_{th} model is added to the RPI Level-15 ATFT model [10] to obtain the composite ΔV_{th} TFT model and was incorporated into the SPICE 3.0 circuit simulator [11] by adding c-language source code.

III. Circuit Example

The performance of the simulator-based a-Si:H TFT ΔV_{th} circuit aging model is demonstrated with a latch circuit shown in Fig. 2. The load transistors (A1–A7) have $W/L = 9\ \mu\text{m}/36\ \mu\text{m}$ and the pull down transistors (A2–A8) have $W/L = 45\ \mu\text{m}/9\ \mu\text{m}$ with $V_{\text{DD}} = 30$ V. The input to the latch (V_{in}) is a 30-V pulse with 4-ms period and a duty cycle of 50%. The clock inputs (O1 and O2) are nonoverlapping 30-V square wave pulses with a 1-ms period and a pulsewidth of 500 μs. The TFTs have an inverted staggered structure with a molybdenum (Mo) gate and a silicon nitride gate dielectric. The source and drain metallization is an aluminum/n+ a-Si:H bilayer. Using the ΔV_{th} model parameters derived from the data used for Fig. 1, the latch is simulated in the ΔV_{th} TFT modified SPICE circuit simulator. The ΔV_{th} of the latch circuit transistors at circuit age periods are listed in the Appendix. Fig. 3 shows that the simulated latch output voltage using the combined ΔV_{th} TFT model closely matches the experimentally measured latch output without stress and after applying V_{GS} bias stress for 1, 2, and 3 h, respectively.

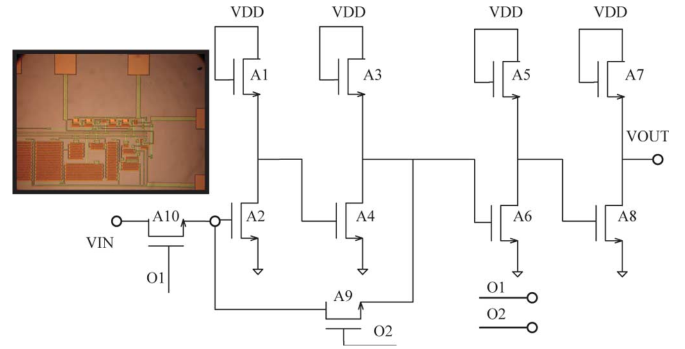

Fig. 2. Latch circuit using n-channel a-Si:H TFTs. The inset shows the latch die photo.

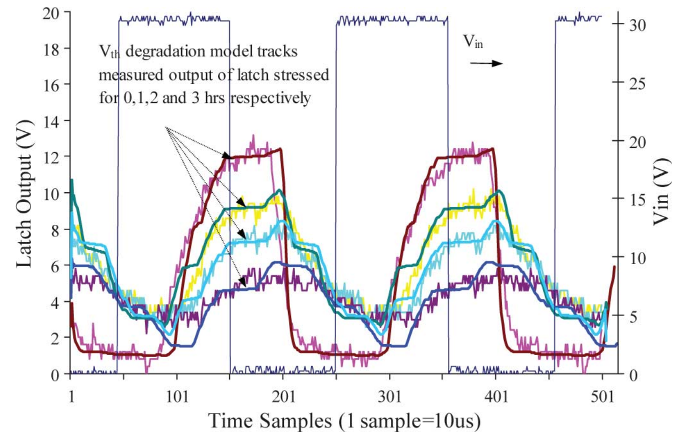

Fig. 3. Simulated and measured latch outputs without stress and after applying stress for 1, 2, and 3 h, respectively.

IV. Conclusion

The least damaged TFT (A5 in Fig. 2) in the latch has a V_{th} degradation of 49% and 64% when stressed for 1 and 3 h, respectively. Lower V_{th} degradation is observed because A5 is always in saturation and has fewer free carriers at the SiN_x/a-Si:H interface. This behavior is correctly predicted by the model. Likewise, latch transistors A10, A2, and A9 exhibit a V_{th} change of 97%, 79%, and 75%, respectively, when stressed for 1 h. The large positive shift is because the transistors are mainly stressed positively even when operating in the inverted mode $(V_{\text{DS}} < 0)$ with $V_{\text{GD}} > 0$. The latch measurements and

TABLE I
ΔV_{th} OF LATCH CIRCUIT AT VARIABLE STRESS PERIODS (t_{age})

Instance	Tage=1 hr	Tage=2 hrs	Tage=3 hrs
A1	2.50	2.97	3.29
A2	3.95	4.70	5.20
A3	2.54	3.03	3.35
A4	3.52	4.18	4.62
A5	2.45	2.91	3.22
A6	3.51	4.17	4.61
A7	2.65	3.15	3.49
A8	3.46	4.12	4.56
A9	3.74	4.44	4.92
A10	4.88	5.80	6.42

simulated results demonstrate that ΔV_{th} model is able to accurately capture V_{th} shifts under different bias stress conditions. The advantage of this implementation is that one can observe the TFT degradation due to gate bias stress for any future time in operation. The present ΔV_{th} model can be improved by including V_{th} degradation effects due to multiple charge trapping mechanisms in the SiN_x/a-Si:H interface region.

APPENDIX

The ΔV_{th} of the latch transistors (A1–A10) obtained from extrapolating the Age parameter of the primary stress run (Table I).

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